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TRANSMITTAL FORM UNDER 37 CFR 1.8 (LARGE ENTITY)

Title: COMPENSATING FOR DIFFERENCES BETWEEN CLOCK SIGNALS

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS

Appellants:	Dormitzer et al.	**APPEAL BRIEF**
Serial No.	09/935,209	
Filing Date	August 22, 2001	
Group Art Unit	2813	
Examiner	Hai L. Nguyen	
Attorney Docket No.	650.232US01 (formerly 100.232US01)	
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1. Introduction

On June 7, 2004, Appellants filed a notice of appeal from the final rejection of claims 1-4, 6-10, 12-15, 17-19, 21, 22, 24-27 and 29-32 set forth in the Office Action mailed April 7, 2004. Three copies of this Appeal Brief are hereby filed on August 9, 2004 and are accompanied by a fee in the amount of $330.00 as required under 37 C.F.R. §1.17(c).

2. Real Party in Interest

The real party in interest in the above-captioned application is BigBand Networks BAS, Inc.

3. Related Appeals and Interferences

There are no other appeals or interferences known to Appellants which will have a bearing on the Board's decision in the present appeal.

4. Status of the Claims

Claims 1-34 are pending in the application and are the subject of this appeal. In office action mailed April 7, 2004, claims 1, 7, 12, 17, 31 and 32 were finally rejected under 35 U.S.C. §102(b) claims 2-4, 6, 8-10, 13-15, 18, 19, 21, 22, 24-27, 29 and 30 were finally rejected under 35 U.S.C. §103(a). Claims 5, 11, 16, 20, 23 and 28 were objected to as being dependent upon a rejected base claim.

5. Status of Amendments

No amendment has been filed subsequent to the Final Office Action mailed April 7, 2004.

6. Summary of the Invention

In one embodiment, a clock compensation circuit 102 is provided in Figure 1. The circuit comprises a clock synchronization circuit 110 coupled to receive an input clock signal 101-1, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals 105. The circuit further comprises a phase comparator 120-1 coupled to receive one of the plurality of internal logic clock signals 105 and a sample clock PHYRET from an associated receiver, wherein the phase comparator 120-1 generates a control signal based on a phase comparison between the sample clock PHYRET and the one of the plurality of internal logic clock signals 105 and a down converter channel 115-1 coupled to receive each of the plurality of internal logic clock signals 105 and the control signal and to pass data PHYDATA in phase with the sample clock PHYRET using the internal logic clock signal on the control signal.

In another embodiment, a clock compensation circuit 102 is provided. The circuit comprises an input for receiving an input clock signal 101-1, a clock synchronization circuit 102 coupled to receive the input clock signal 101-1, wherein the clock signal synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals 105, and a tapped delay line 108 coupled to receive a first one of the plurality of internal logic clock signals to generate a clock signal PHYCLK with a selected delay as an output clock signal. In addition, the circuit includes a phase comparator 120-2 coupled to receive a second one of the plurality of internal logic clock signals 105 and a sample clock SMPCLK from an associated receiver and to generate a control signal based on a phase comparison of the second one of the plurality of internal logic clock signals 105 and the sample clock, and a down converter channel 115-2 coupled to receive the plurality of internal logic clock signals 105 and the control signal and to pass data PHYDATA in phase with the sample clock using the second one of the plurality of internal logic clock signals 105 based on the control signal.

In another embodiment, a method of generating a timing signal is provided. The method includes receiving an input clock signal 101-1, receiving a sample clock from an associated receiver and generating a master clock signal from the input clock signal. The method further includes generating a plurality of internal logic clock signals from the master clock signal and comparing the phase of one of the plurality of internal logic clock signals to the phase of the received sample clock. And, when the one of the plurality of internal logic clock signals is in phase with the received sample clock, selecting a data signal that is clocked on the rising edge of the one of the plurality of internal logic clock signals. Further, when the one of the plurality of internal logic clock signals is out of phase with the received sample clock, selecting the data that is clocked on the falling edge of the one of the plurality of internal logic clock signals. Further more, the method includes passing the selected data signal to the associated receiver.

In an alternate embodiment, a method of generating a timing signal is provided. The method includes receiving an input clock signal, receiving a sample clock from an associated receiver, and generating a master clock signal from the input clock signal. The method further includes generating a plurality of internal logic clock signals from the master clock signal, comparing the phase of the received sample clock, and generating a plurality of delayed clock signals from another one of the plurality of logic clock signals. Each of the plurality of delayed clock signals is synchronized with the sample clock of an associated receiver. Further, when the one of the plurality of internal logic clock signals is in phase with the received sample clock, selecting a data signal that is clocked on the rising edge of the one of the plurality of internal logic clock signals. Further more, when the one of the plurality of internal logic clock signals is out of phase with the received sample clock, selecting the data that is clocked on the falling edge if the one of the plurality of internal logic signals. In addition, the method includes passing the selected data signal to the associated receiver.

7. Issues Presented for Review

The first issue presented in this Appeal is whether the Examiner erred in rejecting claims

1, 7, 12, 17 and 31 under 35 U.S.C. §102(b), as being anticipated by Nishimura et al. (U.S. Patent 5,990,715) (referred to herein as "Nishimura"). A second issue presented in this Appeal is whether the Examiner erred in rejecting claim 32 under 35 U.S.C. §102(b), as being anticipated by Burch et al. (U.S. Patent 5,680,422) (referred to herein as "Burch"). A third issue presented in this Appeal is whether the Examiner erred in rejecting claims 21, 24 and 27 under 35 U.S.C. §103(a), as being unpatentable over Nishimura. A fourth issue presented in this Appeal is whether the Examiner erred in rejecting claim 2-4, 6, 8-10, 13-15, 18, 19, 22, 25, 26, 29 and 30 under 35 U.S.C §103(a) as being unpatentable over Nishimura in view of Riordan et al. (U.S. Patent 5,317,601) (referred to herein as "Riordan").

8. Grouping of Claims

Each of claims 1-32 stands or falls on their own merits for the reasons detailed below. Each of the claims is patentably distinct for the reasons detailed below.

9. Arguments

A. Rejections of claims 1, 7, 12, 17, 31 and 32 under 35 U.S.C. §102 (b)

1. The Applicable Law

35 U.S.C. §102 provides in relevant part:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The

identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbi* test, i.e., identity of terminology is not required. *In re Bond*, 910 F. 2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). *See*, M.P.E.P. 2131.

Anticipation focuses on whether a claim reads on a product or process disclosed in a prior art reference, not on what the reference broadly teaches. *Kalman v. Kimberyl-Clark Corp.,* 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. v. Guardian Industries Corp.,* 75 F.3d 1558, 37 U.S.P.Q.2d 1618 (Fed. Cir. 1996).

2. 35 U.S.C. § 102(b) rejection analysis

The Examiner finally rejected claims 1, 7, 12, 17, 31 and 32 under 35 U.S.C. §102(b) as being anticipated by Nishimura.

Claim 1

Claim 1 is directed to a clock compensation circuit. The clock compensation circuit includes a clock synchronization circuit coupled to receive an input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals. The clock compensation circuit also includes a phase comparator coupled to receive one of the plurality of internal logic clock signals and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the one of the plurality of internal logic clock signals. In addition, the clock compensation circuit includes a down converter channel coupled to receive each of the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the one of the plurality of internal logic clock signals based on the control signal.

In support of this rejection, the final Office Action asserts that "Nishimura discloses in

Fig. 2 an inherent clock compensation circuit, comprising a clock synchronization circuit coupled to receive an input clock signal (1), wherein the clock synchronization circuit generates a master clock signal (S1) and produces a plurality of internal logic clock signals (S2, S3); a phase comparator (31) coupled to receive one (S3) of the plurality of internal logic clock signals and a sample clock (S0) from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample and the one of the plurality of internal logic clock signals; and an inherent down converter channel (32, 33, 34, 41, 51) coupled to receive each of the plurality of internal logic clock signals (S2, S3) and the control signal and to pass data in phase with the sample clock using the one of the plurality of internal logic clock signals based on the control signal." Final Office Action dated 4/7/2004 ¶ 3. Applicant respectfully traverses this rejection.

Applicant respectfully asserts that Nishimura fails to teach or suggest the clock compensation circuit of claim 1. In particular, Nishimura fails to teach "a down converter channel coupled **to receive each of the plurality of internal clock signals** and the control signal". Further, Nishimura fails to teach "to pass data in phase with the sample clock **using one of the plurality of internal logic clock signals based on the control signal**".

Also, the Examiner asserts that items 32, 33, 34, 41 and 51 in Figure 2 of Nishimura inherently teach a down converter channel. Applicant asserts that on the contrary, the detailed description related to items 32, 33, 34, 41 and 51 in Figure 2 of Nishimura (see col. 5 lines 44-51) discusses:

> The delay controller 32 control the delay circuit 33 and the dummy delay circuit 34 to apply the same delay (delay value) in accordance with output signals (comparison result) of the phase comparator 31. Therefore, the delay (delay time) caused by the input circuit 21, delay circuit 33, real line 41, and output circuit 51 are removed, and the internal clock signal for the output circuit 51 is supplied at the same timing of inputting the external clock CLK.

Nishimura does not teach, inherently or otherwise, the limitation **"coupled to receive each of the plurality of internal clock signals and the control signals"**. There is also no

indication in Nishimura to pass data in phase with the sample clock **"using one of the plurality of internal logic clock signals based on the control signal"**. It does not inherently teach or suggest the claimed limitation. The Examiner provides no explanation as to how Nishimura (or any other reference) cures this deficiency.

Furthermore, even assuming, *arguendo*, that items 32, 33, 34, 41 and 51 in figure 2 inherently taught a digital down converter channel, these items would not meet the claimed, "coupled to receive **each of the plurality of internal clock signals** and the control signals." The Examiner asserts that "Nishimura discloses . . . a plurality of **internal clock signals (S2, S3)**." Final Office Action dated 4/7/2004 ¶ 3. However, Nishimura discusses, "a second output signal **(signal S3)** to a first input of the phase comparator 31" and "output signals **(comparison result)** of the phase comparator 31." *Nishimura,* col 5. lines 32-33 and 45-46. Nishimura does not teach or suggest in figure 2 or in any passage that any of elements 32, 33, 34, 41 or 51 receives signal S3. Therefore, even assuming, *arguendo,* that the Examiner's assertions are correct, Nishimura still does not teach or suggest the claimed, "coupled to receive **each of the plurality of internal clock signals** and the control signals."

As a result Nishimura does not anticipate claim 1. Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 1 of the present application under 35 USC § 102(b). The rejection is, therefore, improper and should be withdrawn.

Claims 2-4 and 6

Claims 2-4 and 6 depend from claim 1 and therefore the arguments set forth above with respect to claim 1 also apply to these claims. Claims 2-4 and 6 are allowable for at least the reasons provided above with respect to claim 1.

Claim 7

Claim 7 is directed to a digital down converter. The down converter includes a clock synchronization circuit coupled to receive an input clock signal, wherein the clock

synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals. The down converter also includes a phase comparator coupled to receive one of the plurality of internal logic clock signals and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the one of the plurality of internal logic clock signals. In addition, the down converter also includes a down converter channel coupled to receive each of the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the one of the plurality of internal logic clock signals based on the control signal.

In support of this rejection, the final Office Action provides the same argument as given under claim 1 which asserts that "Nishimura discloses in Fig. 2 an inherent clock compensation circuit, comprising a clock synchronization circuit coupled to receive an input clock signal (1), wherein the clock synchronization circuit generates a master clock signal (S1) and produces a plurality of internal logic clock signals (S2, S3); a phase comparator (31) coupled to receive one (S3) of the plurality of internal logic clock signals and a sample clock (S0) from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample and the one of the plurality of internal logic clock signals; and an inherent down converter channel (32, 33, 34, 41, 51) coupled to receive each of the plurality of internal logic clock signals (S2, S3) and the control signal and to pass data in phase with the sample clock using the one of the plurality of internal logic clock signals based on the control signal." Final Office Action dated 4/7/2004 ¶ 3. Applicant respectfully traverses this rejection.

Applicant respectfully asserts that Nishimura fails to teach or suggest a digital down converter of claim 7. In particular, Nishimura fails to teach "a down converter channel coupled **to receive each of the plurality of internal clock signals** and the control signal". Further, Nishimura fails to teach "to pass data in phase with the sample clock **using one of the plurality of internal logic clock signals based on the control signal**".

Also, the Examiner asserts that 32, 33, 34, 41 and 51 in Figure 2 of Nishimura inherently teach a down converter channel. Applicant respectfully asserts that on the contrary, the detailed

description related to items 32, 33, 34, 41 and 51 in Figure 2 of Nishimura (see col. 5 lines 44-51) specifies:

> The delay controller 32 control the delay circuit 33 and the dummy delay circuit 34 to apply the same delay (delay value) in accordance with output signals (comparison result) of the phase comparator 31. Therefore, the delay (delay time) caused by the input circuit 21, delay circuit 33, real line 41, and output circuit 51 are removed, and the internal clock signal for the output circuit 51 is supplied at the same timing of inputting the external clock CLK.

Nishimura does not teach, inherently or otherwise, the limitation **"coupled to receive each of the plurality of internal clock signals and the control signals"**. There is also no indication in Nishimura to pass data in phase with the sample clock **"using one of the plurality of internal logic clock signals based on the control signal"**. It does not inherently teach or suggest the claimed limitation. The Examiner provides no explanation as to how Nishimura (or any other reference) cures this deficiency.

Furthermore, even assuming, *arguendo*, that items 32, 33, 34, 41 and 51 in figure 2 inherently taught a digital down converter channel, these items would not meet the claimed, "coupled to receive **each of the plurality of internal clock signals** and the control signals." The Examiner asserts that "Nishimura discloses . . . a plurality of **internal clock signals (S2, S3)**." Final Office Action dated 4/7/2004 ¶ 3. However, Nishimura discusses, "a second output signal **(signal S3)** to a first input of the phase comparator 31" and "output signals **(comparison result)** of the phase comparator 31." *Nishimura,* col 5. lines 32-33 and 45-46. Nishimura does not teach or suggest in figure 2 or in any passage that any of elements 32, 33, 34, 41 or 51 receives signal S3. Therefore, even assuming, *arguendo,* that the Examiner's assertions are correct, Nishimura still does not teach or suggest the claimed, "coupled to receive **each of the plurality of internal clock signals** and the control signals."

As a result Nishimura does not anticipate claim 7. Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 7 of the present application under 35 USC § 102(b). The rejection is, therefore, improper and should be withdrawn.

Claims 8-10

Claims 8-10 depend from claim 7 and therefore the arguments set forth above with respect to claim 7 also apply to claims 8-10. Claims 8-10 are allowable for at least the reasons provided above with respect to claim 7.

Claim 12

Claim 12 is directed to a clock compensation circuit. The clock compensation circuit includes an input for receiving an input clock signal and a clock synchronization circuit coupled to receive the input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals. The clock compensation circuit also includes a tapped delay line coupled to receive a first one of the plurality of internal logic clock signals and to generate a clock signal with a selected delay as an output clock signal. In addition, the clock compensation signal includes a phase comparator coupled to receive a second one of the plurality of internal logic clock signals and a sample clock from an associated receiver and to generate a control signal based on a phase comparison of the second one of the plurality of internal logic clock signals and the sample clock. Further, the clock compensation circuit includes a down converter channel coupled to receive the plurality of internal logic clock signals and the control signal and to pass the data in phase with the sample clock using the second one of the plurality of internal logic clock signals based on the control signal.

The Office action asserts that "Nishimura discloses in Fig. 2 an inherent clock compensation circuit, comprising an input (1) for receiving an input clock signal; a clock synchronization circuit (21, 30) coupled to receive the input clock signal, wherein the clock synchronization circuit generates a master clock signal (S1) and produces a plurality of internal clock signals (S2, S3); tapped delay line (34) coupled to receive a first one (S2) of the plurality of internal logic clock signals and to generate a clock signal with a selected delay as an output clock signal; a phase comparator (31) coupled to receive a second one (S3) of the plurality of

internal logic clock signals and a sample clock (S0) from an associated receiver and to generate a control signal based on a phase comparison of the second one of the plurality of internal logic clock signals and the same clock; and a down converter channel (32, 33, 34, 41, 51) coupled to receive the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the second one of the plurality of internal logic clock signals based on the control signal." Final Office Action dated 4/7/2004 ¶ 3. Applicant respectfully traverses this rejection and has carefully reviewed Nishimura and does not find that Nishimura teaches or suggests a clock compensation circuit of claim 12.

Applicant respectfully asserts that Nishimura fails to teach the clock compensation circuit of claim 12. In particular, Nishimura fails to teach "a down converter channel coupled **to receive the plurality of internal logic clock signals** and the control signal". Further, Nishimura fails to teach "to pass data in phase with the sample clock **using the second one of the plurality of internal logic clock signals based on the control signal**".

Also, the Examiner asserts that items 32, 33, 34, 41 and 51 in Figure 2 of Nishimura inherently teach a down converter channel. On the contrary, the detailed description related to items 32, 33, 34, 41 and 51 in Figure 2 of Nishimura (see col. 5 lines 44-51) specifies:

> The delay controller 32 control the delay circuit 33 and the dummy delay circuit 34 to apply the same delay (delay value) in accordance with output signals (comparison result) of the phase comparator 31. Therefore, the delay (delay time) caused by the input circuit 21, delay circuit 33, real line 41, and output circuit 51 are removed, and the internal clock signal for the output circuit 51 is supplied at the same timing of inputting the external clock CLK.

Nishimura does not teach, inherently or otherwise, the limitation **"coupled to receive the plurality of internal clock signals and the control signal"**. There is also no indication in Nishimura to pass data in phase with the sample clock **"using the second one of the plurality of internal logic clock signals based on the control signal"**. It does not inherently teach or suggest the claimed limitation. The Examiner provides no explanation as to how Nishimura (or any other reference) cures this deficiency.

Furthermore, even assuming, *arguendo*, that items 32, 33, 34, 41 and 51 in figure 2 inherently taught a digital down converter channel, these items would not meet the claimed, "coupled to receive **each of the plurality of internal clock signals** and the control signals." The Examiner asserts that "Nishimura discloses . . . a plurality of **internal clock signals (S2, S3)**." Final Office Action dated 4/7/2004 ¶ 3. However, Nishimura discusses, "a second output signal **(signal S3)** to a first input of the phase comparator 31" and "output signals **(comparison result)** of the phase comparator 31." *Nishimura,* col 5. lines 32-33 and 45-46. Nishimura does not teach or suggest in figure 2 or in any passage that any of elements 32, 33, 34, 41 or 51 receives signal S3. Therefore, even assuming, *arguendo,* that the Examiner's assertions are correct, Nishimura still does not teach or suggest the claimed, "coupled to receive **each of the plurality of internal clock signals** and the control signals."

As a result Nishimura does not anticipate claim 12. Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 12 of the present application under 35 USC § 102(b). The rejection is, therefore, improper and should be withdrawn.

Claim 13-15

Claims 13-15 depend from claim 12 and therefore the arguments set forth above with respect to claim 12 also apply to claims 13-15. Claims 13-15 are allowable for at least the reasons provided above with respect to claim 12.

Claim 17

Claim 17 is directed to a clock compensation circuit. The clock compensation circuit includes an input for receiving an input clock signal and a clock synchronization circuit coupled to receive the input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals. The clock compensation circuit also includes a phase comparator coupled to receive a first one of the plurality of internal logic clock signals and a sample clock from an associated receiver and to generate a control

signal based on a phase comparison between the sample clock and the one of the plurality of internal logic clock signals. Additionally, the clock compensation circuit includes a tapped delay line coupled to receive a second one of the plurality of internal logic clock signals and to generate a delayed clock signal for input to the associated receiver, wherein the delayed clock signal is synchronized with the sample clock. Further, the clock compensation circuit includes a down converter channel coupled to receive the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the first one of the plurality of internal logic clock signals based on the control signals.

In support of this rejection, the final Office Action provides the same argument used for claim 12 that asserts that "Nishimura discloses in Fig. 2 an inherent clock compensation circuit, comprising an input (1) for receiving an input clock signal; a clock synchronization circuit (21, 30) coupled to receive the input clock signal, wherein the clock synchronization circuit generates a master clock signal (S1) and produces a plurality of internal clock signals (S2, S3); tapped delay line (34) coupled to receive a first one (S2) of the plurality of internal logic clock signals and to generate a clock signal with a selected delay as an output clock signal; a phase comparator (31) coupled to receive a second one (S3) of the plurality of internal logic clock signals and a sample clock (S0) from an associated receiver and to generate a control signal based on a phase comparison of the second one of the plurality of internal logic clock signals and the same clock; and a down converter channel (32, 33, 34, 41, 51) coupled to receive the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the second one of the plurality of internal logic clock signals based on the control signal." Final Office Action dated 4/7/2004 ¶ 3. Applicant respectfully traverses this rejection and has carefully reviewed Nishimura and does not find that Nishimura teaches or suggests the clock compensation circuit of claim 17.

Applicant respectfully asserts that Nishimura fails to teach the clock compensation circuit of claim 17. In particular, Nishimura fails to teach "a down converter channel coupled **to receive the plurality of internal logic clock signals** and the control signal". Further, Nishimura fails to

teach "to pass the data in phase with the sample clock **using the first one of the plurality of internal logic clock signals based on the control signal**".

Also, the Examiner asserts that items 32, 33, 34, 41 and 51 in Figure 2 of Nishimura inherently teach a down converter channel. On the contrary, the detailed description related to items 32, 33, 34, 41 and 51 in Figure 2 of Nishimura (see col. 5 lines 44-51) specifies:

> The delay controller 32 control the delay circuit 33 and the dummy delay circuit 34 to apply the same delay (delay value) in accordance with output signals (comparison result) of the phase comparator 31. Therefore, the delay (delay time) caused by the input circuit 21, delay circuit 33, real line 41, and output circuit 51 are removed, and the internal clock signal for the output circuit 51 is supplied at the same timing of inputting the external clock CLK.

Nishimura does not teach, inherently or otherwise, the limitation **"coupled to receive the plurality of internal logic clock signals and the control signal"**. There is also no indication in Nishimura that the data is passed in phase with the sample clock **"using the first one of the plurality of internal logic clock signals based on the control signal"**. It does not inherently teach or suggest the claimed limitation. The Examiner provides no explanation as to how Nishimura or any other reference) cures this deficiency.

Furthermore, even assuming, *arguendo*, that items 32, 33, 34, 41 and 51 in figure 2 inherently taught a digital down converter channel, these items would not meet the claimed, "coupled to receive **each of the plurality of internal clock signals** and the control signals." The Examiner asserts that "Nishimura discloses . . . a plurality of **internal clock signals (S2, S3)**." Final Office Action dated 4/7/2004 ¶ 3. However, Nishimura discusses, "a second output signal (**signal S3**) to a first input of the phase comparator 31" and "output signals (**comparison result**) of the phase comparator 31." *Nishimura,* col 5. lines 32-33 and 45-46. Nishimura does not teach or suggest in figure 2 or in any passage that any of elements 32, 33, 34, 41 or 51 receives signal S3. Therefore, even assuming, *arguendo,* that the Examiner's assertions are correct, Nishimura still does not teach or suggest the claimed, "coupled to receive **each of the plurality of internal clock signals** and the control signals."

As a result Nishimura does not anticipate claim 17. Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 17 of the present application under 35 USC § 102(b). The rejection is, therefore, improper and should be withdrawn.

Claim 18, 19

Claims 18 and 19 depend from claim 17 and therefore the arguments set forth above with respect to claim 17 also apply to these claims. Claims 18 and 19 are allowable for at least the reasons provided above with respect to claim 17.

Claim 31

Claim 31 is directed to a clock compensation circuit. The clock compensation circuit includes a phase comparator coupled to receive a first clock signal and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the first clock signal. In addition, the clock compensation circuit includes a data channel coupled to receive the first clock signal and the control signal and to pass data in phase with the sample clock using the first clock signal based on the control signal.

In support of this rejection, the final Office Action provides the same argument used for claim 1 that asserts that "Nishimura discloses in Fig. 2 an inherent clock compensation circuit, comprising a clock synchronization circuit coupled to receive an input clock signal (1), wherein the clock synchronization circuit generates a master clock signal (S1) and produces a plurality of internal logic clock signals (S2, S3); a phase comparator (31) coupled to receive one (S3) of the plurality of internal logic clock signals and a sample clock (S0) from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample and the one of the plurality of internal logic clock signals; and an inherent down converter channel (32, 33, 34, 41, 51) coupled to receive each of the plurality of internal logic clock signals (S2, S3) and the control signal and to pass data in phase with the sample clock using the one of the plurality of internal logic clock signals based on the control signal." Final

Office Action dated 4/7/2004 ¶ 3. Applicant respectfully traverses this rejection.

As provided in the arguments with respect to claim 1, the Applicant respectfully asserts that Nishimura fails to teach the clock compensation circuit of claim 31. In particular, Nishimura fails to teach a data channel coupled to receive the first clock signal and the control signal and to pass data in phase with the sample clock **using the first clock signal based on the control signal**. As a result Nishimura does not anticipate claim 31.

Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 31 of the present application under 35 USC § 102(b). The rejection is, therefore, improper and should be withdrawn.

Claim 32

Claim 32 is directed to a clock compensation circuit. The clock compensation circuit includes a phase alignment circuit which includes a phase comparator coupled to receive a first clock signal and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the first clock signal. In addition, the phase alignment circuit includes a multiplexer to receive first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal.

In support of this rejection, the final Office Action asserts that "Burch et al. discloses in Fig. 3 an inherent clock compensation circuit comprising an inherent phase alignment circuit which includes a phase comparator (56) coupled to receive a first clock signal (54) and a sample clock (59) from an associated receiver wherein the phase comparator generates a control signal (60); and a multiplexer to receive first and second data signals (57, 72) and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample

clock signal (see column 2, lines 21-65)." Final Office Action dated 4/7/2004 ¶ 4. Applicant respectfully traverses this rejection.

Applicant asserts that Burch fails to teach the clock compensation circuit of claim 32. In particular, Burch does not teach "a phase comparator coupled to receive a first clock signal and a sample clock signal ***from an associated receiver.***" Additionally, Burch fails to teach "the ***phase comparator*** generates a control signal ***based on a phase comparison*** between the sample clock and the first clock signal." Furthermore, Burch fails to teach "the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal ***such that*** the data signal passed by the multiplexer is in phase with the sample clock signal."

Burch discusses, "[t]he read clock 59 and the write clock 54 are input to a phase comparator 56." *Burch,* col. 2 lines 36-37. Burch does not disclose receiving "a sample clock from an associated receiver." Burch also discusses, "a phase comparator 56, which provides a binary output 60 to ***a control logic unit*** 65. ***Control logic unit*** 65 receives the output of phase comparator 60, a synchronized clock 63 produced by a clock generator 64, and optionally, a delayed frame sync signal 58 from the frame aligned elastic store 55, and ***generates a control signal*** 66 to multiplexer 61." *Id.* at lines 37-43. Burch does not disclose that "the ***phase comparator*** generates a control signal" as disclosed in claim 32. Burch discusses, "a binary output 60" and "a control signal 66" but Applicant does not find that it discloses "a control signal 60" as asserted by the Examiner.

In addition, Burch discusses, "Control logic unit 65 directs multiplexer 61 to switch between the synchronized data signal 57 and the other data signal 72, ***based on a predefined stuffing frame format.***" *Id.* at lines 59-61. Burch does not disclose "a control signal ***based on a phase comparison"*** as found in claim 32.

Finally, Burch discusses, "multiplexer 66 switches the data line 62 between the ***synchronized*** data signal 57, the other data signal 72, and the stuffing pulse data signal 68." *Id.* at lines 48-51. Burch further discusses, "The `other data` unit 70 represents memory used to

store synchronization, maintenance, monitoring, and other various data that is ***incorporated into*** the synchronized data output stream 62." *Id.* at 54-57. Burch does not disclose "selectively outputting either the first data signal or the second data signal based on the control signal ***such that*** the data signal passed by the multiplexer is in phase."

As a result Burch does not anticipate claim 32. Accordingly, it is respectfully submitted that the Examiner erred in rejecting claim 32 of the present application under 35 USC § 102(b). The rejection is, therefore, improper and should be withdrawn.

B. Rejection of claims 2-4, 6, 8-10, 13-15, 18, 19, 21, 22, 24-27, 29 and 30 under 35 U.S.C. §103(a)

1. Applicable Law

35 U.S.C.§ 103 provides in relevant part:

Conditions for patentability; non-obvious subject matter.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

To establish a case of *prima facie* obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based in the applicant's

disclosure. *In re vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir 1991). MPEP § 2143 - § 2143.03.

2. 35 U.S.C. § 103(a) Rejection Analysis

The Examiner finally rejected claims 2-4, 6, 8-10, 13-15, 18, 19, 22, 24-27, 29 and 30 under 35 U.S.C. §103(a) as being unpatentable over US Patent No. 5,990,715 (Nishimura) in view of US Patent No. 5,317,601 (Riordan).

The Examiner finally rejected claims 21, 24, and 27 under 35 U.S.C> §103(a) as being unpatentable over Nishimura.

Claim 2-4 and 6

As mentioned earlier under the section for 35 U.S.C. § 102(b) rejection analysis, claims 2-4 and 6 are dependant claims of claim 1 and therefore the arguments set forth with respect to claim 1 also apply to claims 2-4 and 6. Also, Riordan does not teach "a down converter channel coupled **to receive each of the plurality of internal clock signals and the control signal**". Further, Riordan fails to teach "to pass data in phase with the sample clock **using one of the plurality of internal logic clock signals based on the control signal.**" As Nishimura does not anticipate claim 1 and Riordan does not cure the deficiency in Nishimura, the examiner has failed to establish a prima facie case of obviousness with respect to claims 2-4 and 6 since Nishimura and Riordan either alone or in combination do not teach or suggest all the claim limitations of claims 2-4 and 6. Therefore, the rejection is improper and should be withdrawn. Claims 2-4 and 6 are allowable.

Claims 8-10

As mentioned earlier under the section for 35 U.S.C. § 102(b) rejection analysis, claims 8-10 are dependant claims of claim 7 and therefore the arguments set forth with respect to claim 7 also apply to claims 8-10. Also, Riordan does not teach "a down converter channel coupled **to receive each of the plurality of internal clock signals and the control signal**". Further,

Riordan fails to teach "to pass data in phase with the sample clock **using one of the plurality of internal logic clock signals based on the control signal.**" As Nishimura does not anticipate claim 7 and Riordan does not cure the deficiency in Nishimura, the examiner has failed to establish a prima facie case of obviousness with respect to claims 8-10 since Nishimura and Riordan either alone or in combination do not teach or suggest all the claim limitations of claims 8-10. Therefore, the rejection is improper and should be withdrawn. Claims 8-10 are allowable.

Claims 13-15

As mentioned earlier under the section for 35 U.S.C. § 102(b) rejection analysis, claims 13-15 are dependant claims of claim 12 and therefore the arguments set forth with respect to claim 12 also apply to claims 13-15. Also, Riordan does not teach "a down converter channel coupled **to receive the plurality of internal clock signals and the control signal**". Further, Riordan fails to teach "to pass data in phase with the sample clock **using the second one of the plurality of internal logic clock signals based on the control signal.**" As Nishimura does not anticipate claim 12 and Riordan does not cure the deficiency in Nishimura, the examiner has failed to establish a prima facie case of obviousness with respect to claims 13-15 since Nishimura and Riordan either alone or in combination do not teach or suggest all the claim limitations of claims 13-15. Therefore, the rejection is improper and should be withdrawn. Claims 13-15 are allowable.

Claims 18 and 19

As mentioned earlier under the section for 35 U.S.C. § 102(b) rejection analysis, claims 18 and 19 are dependant claims of claim 17 and therefore the arguments set forth with respect to claim 17 also apply to claims 18 and 19. Also, Riordan does not teach "a down converter channel coupled **to receive the plurality of internal clock signals and the control signal**". Further, Riordan fails to teach "to pass data in phase with the sample clock **using the first one of the plurality of internal logic clock signals based on the control signal.**" As Nishimura does not anticipate claim 17 and Riordan does not cure the deficiency in Nishimura, the examiner has

failed to establish a prima facie case of obviousness with respect to claims 18 and 19 since Nishimura and Riordan either alone or in combination do not teach or suggest all the claim limitations of claims 18 and 19. Therefore, the rejection is improper and should be withdrawn. Claims 18 and 19 are allowable.

Claims 21

Claim 21 is directed to a communication system. The communication system includes a plurality of receivers, wherein each receiver is coupled to receive a data signal and a clock signal. The communication system also includes a digital down conversion circuit that includes a clock synchronization circuit coupled to receive an input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals. The digital down conversion circuit also includes, a plurality of phase comparators, wherein each phase comparator is coupled to receive a first one of the plurality of internal logic clock signals and a sample clock signal from an associated one of the plurality of receivers and to generate a control signal based on a comparison of the phase of the first one of the plurality of internal logic clock signals with the sample clock signal. In addition, the digital down conversion circuit includes a plurality of down converter channels, wherein each of the plurality of down converter channels is coupled to receive the plurality of internal logic clock signals and the control signal and passes data from the data signal in phase with the sample clock signal.

In support of this rejection, the Examiner in the final Office Action asserts that "Nishimura meets all of the claimed limitations except that Nishimura discloses only one set of the circuit instead of a plurality as called for in claim 21. It would have been obvious to one of ordinary skill in the art to duplicate the clock compensation circuit taught by Nishimura for providing a synchronous system that is required more than one circuit module." Final Office Action dated 4/7/2004 ¶ 6.

Applicant respectfully traverses the Examiner's rejection. Claim 21 is not taught or

suggested by Nishimura. In particular, Nishimura does not teach or suggest "wherein each of the plurality of down converter channels is coupled to receive the plurality of internal logic clock signals" as found in claim 21. Further, as discussed above with respect to claim 1, Nishimura does not teach or suggest a "down converter channel" as disclosed. Duplication of the circuit elements discussed in Nishimura will not cure this deficiency nor will duplication meet the claimed "plurality of down converter channels." Therefore, since Nishimura does not teach or suggest every element in claim 21, claim 21 is not obvious over Nishimura. Applicant respectfully requests the withdrawal of claim 21 under 35 USC §103(a).

Claims 22-24

Claims 22-24 depend from claim 21 and further define patentably distinct claim 21. Therefore, the arguments set forth above with respect to claim 21 also apply to claims 22-24. Claims 22-24 are allowable for at least the reasons provided above with respect to claim 21.

Claims 27

Claim 27 is directed to a communication system. The communication system includes a plurality of analog to digital converters. The communication system also includes a digital down converter coupled to receive an input clock signal from one of the plurality of analog to digital converters, wherein the digital down converter includes a clock synchronization circuit coupled to receive the input clock signal and to generate a master clock signal and a plurality of internal logic clock signals. The down converter also includes a plurality of phase comparators, wherein each phase comparator is coupled to receive a first one of the plurality of internal logic clock signals and a sample clock from an associated receiver, and wherein each phase comparator generates a control signal based on a phase comparison between the sample clock and the first one of the plurality of internal logic clock signals. In addition, the down converter includes a plurality of down converter channels, wherein each down converter channel is coupled to receive each of the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the first one of the plurality of internal logic clock signals based on the control signal. The communication system also includes a plurality of receivers,

each associated with one of the plurality of phase comparators and one of the plurality of down converter channels; and a tapped delay line coupled to a second one of the plurality of internal logic clock signals and to generate a clock signal with a selected delay as an output clock signal for each of the plurality of receivers.

In support of this rejection, the Examiner in the final Office Action asserts that "Nishimura meets all of the claimed limitations except that Nishimura discloses only one set of the circuit instead of a plurality as called for in claim 2[7]. It would have been obvious to one of ordinary skill in the art to duplicate the clock compensation circuit taught by Nishimura for providing a synchronous system that is required more than one circuit module." Final Office Action dated 4/7/2004 ¶ 6. Applicant respectfully traverses this rejection.

Applicant respectfully traverses the Examiner's rejection. Claim 27 is not taught or suggested by Nishimura. In particular, Nishimura does not teach or suggest "wherein each of the plurality of down converter channels is coupled to receive the plurality of internal logic clock signals" as found in claim 27. Further, as discussed above with respect to claim 1, Nishimura does not teach or suggest a "down converter channel" as disclosed. Duplication of the circuit elements discussed in Nishimura will not cure this deficiency nor will duplication meet the claimed "plurality of down converter channels." Therefore, since Nishimura does not teach or suggest every element in claim 21, claim 21 is not obvious over Nishimura. Applicant respectfully requests the withdrawal of claim 21 under 35 USC §103(a).

Claim 29

Claim 29 depends from claim 27 and further defines patentably distinct claim 27. Therefore, the arguments set forth above with respect to claim 27 also apply to claim 29. Claim 29 is allowable for at least the reasons provided above with respect to claim 27.

Claim 30

Claim 30 is directed to a clock compensation circuit. The clock compensation circuit includes a clock synchronization circuit coupled to receive an input clock signal, wherein the

clock synchronization circuit generates a plurality of internal logic clock signal of different frequencies; and a phase comparator coupled to receive at least one of the internal logic clock signal and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the least one internal logic clock signal. The clock compensation circuit also includes a down converter channel coupled to receive the at least one internal logic clock signal and the control signal and to pass data in phase with the sample clock using the internal logic clock signal based on the control signal.

In support of this rejection, the final Office Action asserts that "Nishimura meets all of the claimed limitations except that the plurality of internal logic clock signals (S2, S3) of Nishimura are not different frequencies. Riordan et al. teaches in Fig. 2 a synchronization circuit generates a plurality of internal logic clock signals of different frequencies (PLL1x, 1x, 2x, 4x, Sync4x) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement that teaching with the prior art (Fig. 2 of Nishimura) to generate a plurality of internal logic clock signals of different frequencies in order to provide a number of precisely synchronized clock signals having different frequencies to meet the demand of many different functional portions of the circuit." Final Office Action dated 4/7/2004 ¶ 8. Applicant respectfully traverses the Examiner's rejection of claim 30 under 103(a).

Applicant asserts that in addition to not meeting the element of a plurality of internal logic clock signal of different frequencies, as acknowledged by the Examiner, Nishimura also does not meet all of the other elements of claim 30. In particular, Nishimura does not teach or suggest, "a phase comparator coupled to receive at least one of the internal logic clock signal and a sample clock ***from an associated receiver***." The Examiner asserts that this claim element is met by "a phase comparator (31) couple to receive ***one (S3) of the plurality of internal logic*** clock signals and a ***sample clock (S0)*** from an associated receiver." Final Office Action dated 4/7/2004 ¶ 3. The Examiner also asserts that "Nishimura discloses . . . a plurality of ***internal***

clock signals (S2, S3)." *Id.* Applicant asserts that contrary to the Examiner's assertion, Nishimura discusses, "the divider circuit 30 ***supplies a first output signal (signal S2)*** to the dummy delay circuit 34, and also supplies ***a second output signal (signal S3)***. Note that ***the first output signal (S2)*** of the divider circuit 30 ***is supplied to a second input (signal S0)*** of the phase comparator 31." *Nishimura,* col. 5 lines 29-34. Nishimura further discusses, "***the signal S0***, which is supplied to another input (second input) of the phase comparator 31, ***is a signal corresponding to the first output signal S2*** delayed by the dummy delay circuit 34, dummy line 42, dummy out-put circuit 52, and dummy input circuit 22." *Nishimura,* col. 6 lines 52-57. Nishimura does not teach or suggest "a sample clock ***from an associated receiver"*** as disclosed in claim 30. Additionally, as discussed above with respect to claim 1, Nishimura does not teach or suggest, "a down converter channel coupled to receive the at least one internal logic clock signal and the control signal and to pass data in phase with the sample clock ***using the internal logic clock signal based on the control signal***." Therefore, as discussed above with respect to claims 2-4 and 6, since Nishimura and Riordan, either alone or in combination, do not teach or suggest all the claim limitations of claim 30, claim 30 is not obvious over Nishimura in view of Riordan. Therefore, the rejection is improper and should be withdrawn.

Furthermore, Applicant respectfully traverses the Examiner's asserted motivation for combining Nishimura and Riordan. to modify Nishimura. Applicant asserts that there is nothing in Nishimura which discloses or suggests a "demand of many different functional portions of the circuit" that "a number of precisely synchronized clock signals having different frequencies" would meet, as asserted by the Examiner. Final Office Action dated 4/7/2004 ¶ 8. Hence, one of ordinary skill in the art would not be motivated to combine Riordan with Nishimura to "generate[] a plurality of internal logic clock signal of different frequencies." Furthermore, Nishimura discusses, "***the divider circuit*** 30 receives the signal S1 (external clock CLK) which is the output signal of the input circuit 21, and ***generates a signal S2*** (first output signal) having a clock cycle corresponding to eight clock cycles of the external clock CLK ***and a signal S3 (second output signal) which is an inverted signal of the signal S2***." *Nishimura*, col. 6 lines

38-43. Assuming, *arguendo*, that the Examiner is correct in asserting that "Nishimura discloses . . . a plurality of ***internal clock signals (S2, S3)***", there is still no suggestion or indication in Nishimura of a problem with using "a signal S3 (second output signal) which is an inverted signal of the signal S2" that needs to be addressed by Riordan to modify Nishimura with "internal logic clock signal of different frequencies." Therefore, since there is no motivation to combine the two references, claim 30 is not obvious over Nishimura in view of Riordan. Accordingly, the Applicant respectfully requests the withdrawal of the rejections of Claim 30 under 103(a).

10. Summary

Appellants have set forth reasons why the Examiner is incorrect in maintaining the rejections of the pending claims. Specifically, the Examiner has failed to set forth a prima facie case of anticipation or obviousness. Nishimura, Riordan and Burch either alone or in combination do not teach all of the limitations in the pending independent and dependant claims. Appellant respectfully submits that, for the above reasons, Claims 1-32 are allowable over the cited art. Therefore, reversal of the Examiner's rejections is respectfully requested.

Respectfully submitted,

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Appendix 1

The Claims on Appeal

1. A clock compensation circuit, comprising:

a clock synchronization circuit coupled to receive an input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals;

a phase comparator coupled to receive one of the plurality of internal logic clock signals and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the one of the plurality of internal logic clock signals; and

a down converter channel coupled to receive each of the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the one of the plurality of internal logic clock signals based on the control signal.

2. The clock compensation circuit of claim 1, wherein the clock synchronization circuit comprises:

a phase-locked loop coupled to receive the input clock signal and to generate the master clock signal; and

a clock divider coupled to receive the master clock signal and to produce the plurality of internal logic clock signals.

3. The clock compensation circuit of claim 1, wherein the one of the plurality of internal logic clock signals is matched in frequency to the sample clock.

4. The clock compensation circuit of claim 1, wherein the synchronization circuit receives an input clock signal on the order of 100 MHz and produces internal logic clock signals on the

order of 20 MHz, 40 MHz, and 100 MHz.

5. The clock compensation circuit of claim 1, wherein the down converter channel comprises:

a first flip flop circuit coupled to receive the one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal.

6. The clock compensation circuit of claim 1, wherein the down converter channel produces two selectable outputs that are 180 degrees out of phase.

7. A digital down converter, comprising:

a clock compensation circuit including:

a clock synchronization circuit coupled to receive an input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals;

a phase comparator coupled to receive one of the plurality of internal logic clock signals and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the one of the plurality of internal logic clock signals; and

a down converter channel coupled to receive each of the plurality of internal logic

clock signals and the control signal and to pass data in phase with the sample clock using the one of the plurality of internal logic clock signals based on the control signal.

8. The digital down converter of claim 7, wherein the clock synchronization circuit comprises:

a phase-locked loop coupled to receive the input clock signal and to generate the master clock signal; and

a clock divider coupled to receive the master clock signal and to produce the plurality of internal logic clock signals.

9. The digital down converter of claim 7, wherein the one of the plurality of internal logic clock signals is matched in frequency to the sample clock.

10. The digital down converter of claim 7, wherein the synchronization circuit receives an input clock signal on the order of 100 MHz and produces internal logic clock signals on the order of 20 MHz, 40 MHz, and 100 MHz.

11. The digital down converter of claim 7, wherein the down converter channel comprises:

a first flip flop circuit coupled to receive the one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal.

12. A clock compensation circuit, comprising:

an input for receiving an input clock signal;

a clock synchronization circuit coupled to receive the input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals;

a tapped delay line coupled to receive a first one of the plurality of internal logic clock signals and to generate a clock signal with a selected delay as an output clock signal;

a phase comparator coupled to receive a second one of the plurality of internal logic clock signals and a sample clock from an associated receiver and to generate a control signal based on a phase comparison of the second one of the plurality of internal logic clock signals and the sample clock; and

a down converter channel coupled to receive the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the second one of the plurality of internal logic clock signals based on the control signal.

13. The clock compensation circuit of claim 12, wherein the clock synchronization circuit comprises:

a phase-locked loop coupled to receive the input clock signal and to generate the master clock signal; and

a clock divider coupled to receive the master clock signal and to produce the plurality of internal logic clock signals.

14. The clock compensation circuit of claim 12, wherein the clock divider receives a master clock signal on the order of 200 MHz and produces internal logic clock signals on the order of 20 MHz, 40 MHz, and 100 MHz.

15. The clock compensation circuit of claim 12, wherein the second one of the plurality of internal logic clock signals is matched in frequency to the sample clock.

16. The clock compensation circuit of claim 12, wherein the down converter channel comprises:

a first flip flop circuit coupled to receive the second one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the second one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal.

17. A clock compensation circuit, comprising:

an input for receiving an input clock signal;

a clock synchronization circuit coupled to receive the input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals;

a phase comparator coupled to receive a first one of the plurality of internal logic clock signals and a sample clock from an associated receiver and to generate a control signal based on a phase comparison between the sample clock and the one of the plurality of internal logic clock signals;

a tapped delay line coupled to receive a second one of the plurality of internal logic clock signals and to generate a delayed clock signal for input to the associated receiver, wherein the delayed clock signal is synchronized with the sample clock; and

a down converter channel coupled to receive the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the first one of the plurality of internal logic clock signals based on the control signal.

18. The clock compensation circuit of claim 17, wherein the clock synchronization circuit comprises:

a phase-locked loop coupled to receive the input clock signal and to generate the master clock signal; and

a clock divider coupled to receive the master clock signal and to produce the plurality of internal logic clock signals.

19. The clock compensation circuit of claim 17, wherein the first one of the plurality of internal logic clock signals is matched in frequency to the sample clock.

20. The clock compensation circuit of claim 17, wherein the down converter channel comprises:

a first flip flop circuit coupled to receive the first one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the first one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop circuit; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal.

21. A communications system, comprising:

a plurality of receivers, wherein each receiver is coupled to receive a data signal and a clock signal;

a digital down conversion circuit, including:

a clock synchronization circuit coupled to receive an input clock signal, wherein the clock synchronization circuit generates a master clock signal and produces a plurality of internal logic clock signals;

a plurality of phase comparators, wherein each phase comparator is coupled to receive a first one of the plurality of internal logic clock signals and a sample clock signal from an associated one of the plurality of receivers and to generate a control signal based on a comparison of the phase of the first one of the plurality of internal logic clock signals with the sample clock signal; and

a plurality of down converter channels, wherein each of the plurality of down converter channels is coupled to receive the plurality of internal logic clock signals and the control signal and passes data from the data signal in phase with the sample clock signal.

22. The communications system of claim 21, wherein the synchronization circuit comprises:

a phase-locked loop coupled to receive the input clock signal and to generate the master clock signal therefrom; and

a clock divider coupled to receive the master clock signal and to produce the plurality of internal logic clock signals therefrom.

23. The communications system of claim 21, wherein each of the down converter channels comprises:

a first flip flop circuit coupled to receive the first one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the first one of the plurality of internal logic

clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop circuit; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed is in phase with the sample clock signal.

24. The communications system of claim 21, further comprising a tapped delay line coupled to receive a second one of the plurality of internal logic clock signals and to generate a plurality of output clock signals with a selected delay based on the second one of the plurality of internal logic clock signals, wherein each of the plurality of output clock signals is used by the associated receiver to generate the sample clock.

25. A method of generating a timing signal, the method comprising:

receiving an input clock signal;

receiving a sample clock from an associated receiver;

generating a master clock signal from the input clock signal;

generating a plurality of internal logic clock signals from the master clock signal;

comparing the phase of one of the plurality of internal logic clock signals to the phase of the received sample clock;

when the one of the plurality of internal logic clock signals is in phase with the received sample clock, selecting a data signal that is clocked on the rising edge of the one of the plurality of internal logic clock signals;

when the one of the plurality of internal logic clock signals is out of phase with the received sample clock, selecting the data that is clocked on the falling edge of the one of the plurality of internal logic clock signals; and

passing the selected data signal to the associated receiver.

26. A method of generating a timing signal, comprising:

receiving an input clock signal;

receiving a sample clock from an associated receiver;

generating a master clock signal from the input clock signal;

generating a plurality of internal logic clock signals from the master clock signal;

comparing the phase of one of the plurality of internal logic clock signals to the phase of the received sample clock;

generating a plurality of delayed clock signals from another one of the plurality of logic clock signals, wherein each of the plurality of delayed clock signals is synchronized with the sample clock of an associated receiver;

when the one of the plurality of internal logic clock signals is in phase with the received sample clock, selecting a data signal that is clocked on the rising edge of the one of the plurality of internal logic clock signals;

when the one of the plurality of internal logic clock signals is out of phase with the received sample clock, selecting the data that is clocked on the falling edge of the one of the plurality of internal logic clock signals; and

passing the selected data signal to the associated receiver.

27. A communications system, comprising:

a plurality of analog to digital converters;

a digital down converter coupled to receive an input clock signal from one of the plurality of analog to digital converters, wherein the digital down converter includes:

a clock synchronization circuit coupled to receive the input clock signal and to generate a master clock signal and a plurality of internal logic clock signals;

a plurality of phase comparators, wherein each phase comparator is coupled to receive a first one of the plurality of internal logic clock signals and a sample clock from an associated receiver, and wherein each phase comparator generates a

control signal based on a phase comparison between the sample clock and the first one of the plurality of internal logic clock signals;

a plurality of down converter channels, wherein each down converter channel is coupled to receive each of the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the first one of the plurality of internal logic clock signals based on the control signal;

a plurality of receivers, each receiver associated with one of the plurality of phase comparators and one of the plurality of down converter channels; and

a tapped delay line coupled to a second one of the plurality of internal logic clock signals and to generate a clock signal with a selected delay as an output clock signal for each of the plurality of receivers.

28. The system of claim 27, wherein each of the plurality of down converter channels comprises:

a first flip flop circuit coupled to receive the first one of the plurality of internal logic clock signals and to pass a first data signal with a first phase;

a second flip flop circuit coupled to receive the first one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop circuit; and

a multiplexer coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed is in phase with the sample clock signal.

29. The system of claim 27, wherein each of the clock synchronization circuits comprises:

a phase-locked loop coupled to receive the input clock signal and to generate the master clock signal; and

a clock divider coupled to receive the master clock signal and to produce the plurality of

internal logic clock signals.

30. A clock compensation circuit, comprising:

a clock synchronization circuit coupled to receive an input clock signal, wherein the clock synchronization circuit generates a plurality of internal logic clock signal of different frequencies;

a phase comparator coupled to receive at least one of the internal logic clock signal and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the at least one internal logic clock signal; and

a down converter channel coupled to receive the at least one internal logic clock signal and the control signal and to pass data in phase with the sample clock using the internal logic clock signal based on the control signal.

31. A clock compensation circuit, comprising:

a phase comparator coupled to receive a first clock signal and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the first clock signal; and

a data channel coupled to receive the first clock signal and the control signal and to pass data in phase with the sample clock using the first clock signal based on the control signal.

32. A clock compensation circuit, comprising:

a phase alignment circuit which includes:

a phase comparator coupled to receive a first clock signal and a sample clock from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the first clock signal; and

a multiplexer to receive first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal.